Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; ~~and~~

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 2 (Original): A semiconductor memory according to claim 1, wherein materials of said floating gate electrode and a channel region between said pair of impurity doped regions are selected so that a Fermi level of said floating gate electrode is in a forbidden band of the channel region when an external voltage is not applied between the channel region and said first control gate electrode.

Claim 3 (Canceled).

Claim 4 (Withdrawn): A semiconductor memory according to claim 1, further comprising:

an element isolation insulating film formed on a partial surface area of said semiconductor substrate and surrounding said pair of impurity doped regions and a channel region between said pair of impurity doped regions,

wherein said floating gate electrode and said first control gate electrode extend on said element isolation insulating film, said gate insulating film covers upper and side surfaces of said floating gate electrode on said element isolation insulating film, and said first control gate

electrode faces the upper and side surfaces of said floating gate electrode on said element isolation insulating film via said gate insulating film.

Claim 5 (Withdrawn): A semiconductor memory according to claim 1, wherein the side wall of said floating gate electrode curves so that said floating gate electrode widens as a height thereof from the surface of said semiconductor substrate becomes large.

Claim 6 (Withdrawn): A method of manufacturing a semiconductor memory, comprising the steps of:

forming a tunneling insulating film on a surface of a semiconductor substrate, the tunneling film having a thinness enough to transmit carriers therethrough by a tunneling phenomenon;

forming a first conductive film on the tunneling insulating film, the first conductive film being made of conductive material or semiconductor material;

forming a dielectric film on the first conductive film, the dielectric film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

forming a second conductive film on the dielectric film, the second conductive film being made of conductive material or semiconductor material;

patterning a lamination structure from an upper surface of the second conductive film to at least a lower surface of the first conductive film to leave a laminated mesa including the first conductive film, the dielectric film and the second conductive film;

forming a gate insulating film covering upper and side surfaces of the laminated mesa and a partial surface of the semiconductor substrate on both sides of the laminated mesa, the gate

insulating film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

forming a third conductive film covering a whole surface of the gate insulating film, the third conductive film being made of conductive material or semiconductor material;

anisotropically etching the third conductive film to leave a side control gate electrode made of the third conductive film over a side wall of the laminated mesa;

doping impurities in a surface layer of the semiconductor substrate on both sides of a gate structure including the laminated mesa and the side control gate electrode to form impurity doped regions; and

electrically connecting the side control gate electrode to the second conductive film constituting the laminated mesa.

Claim 7 (Withdrawn): A method of manufacturing a semiconductor memory, comprising the steps of:

forming an element separation insulating film on a surface of a semiconductor substrate to define an active region surrounded with the element separation insulating film;

forming a tunneling insulating film on the active region, the tunneling insulating film having a thinness enough to transmit carriers therethrough by a tunneling phenomenon;

forming a first conductive member on the tunneling insulating film, the first conductive film traversing the active region and made of conductive material or semiconductor material;

forming a gate insulating film on upper and side surfaces of the first conductive member and on a partial area of the active region on both sides of the first conductive member, the gate

insulating film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

covering a surface of the gate insulating film with a conductive film made of conductive material or semiconductor material;

anisotropically etching the conductive film to leave a side control gate electrode made of the conductive film over a side wall of the first conductive member; and

doping impurities in a surface layer of the active region on both sides of a gate structure including the first conductive member and the side control gate electrode.

Claim 8 (Withdrawn): A method of manufacturing a semiconductor memory according to claim 7, wherein:

in said step of forming the first conductive member the first conductive member is formed to extend on the element separation insulating film; and

in said step of leaving the side control gate electrode the conductive film is left over upper and side surfaces of the first conductive member on the element separation insulating film.

Claim 9 (Withdrawn): A method of manufacturing a semiconductor memory, comprising the steps of:

forming an element separation insulating film on a surface of a semiconductor substrate to define an active region surrounded with the element separation insulating film;

forming a first film over the whole surface of the semiconductor substrate;

forming an opening through the first film, the opening traversing the active region;

forming a gate insulating film on a surface of the active region exposed on a bottom of the opening, the gate insulating film having a thickness not allowing carriers to transmit therethrough by tunneling phenomena;

forming a second film on bottom and side surfaces of the opening and on an upper surface of the first film, the second film being made of conductive material or semiconductor material;

anisotropically etching the second film to leave side control gate electrode of the second film on the side surfaces of the opening and to expose a surface of the active region in a central area of the bottom of the opening;

forming a tunneling insulating film on the exposed surface of the active region, the tunneling insulating film having a thinness enough to transmit carriers therethrough by the tunneling phenomenon, and forming a dielectric film on a side wall of the side control gate electrode, the dielectric film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

forming a third film burying the opening and covering an upper surface of the first film, the third film being made of conductive material or semiconductor material;

etching back the third film to remove the third film on the first film and to leave a floating gate electrode of the third film in the opening;

removing the first film; and

doping impurities in a surface layer of the active region on both sides of a gate structure including the side control gate electrode and the floating gate electrode.

Claim 10 (Withdrawn): A method of manufacturing a semiconductor memory, comprising the steps of:

forming an element separation insulating film on a surface of a semiconductor substrate to define an active region surrounded with the element separation insulating film;

forming a dummy gate electrode on the active region, the dummy gate electrode traversing the active region;

doping impurities in a surface layer of the active region on both sides of the dummy electrode;

forming a first film over the semiconductor substrate, the first film covering the dummy gate electrode;

removing the first film on an upper surface of the dummy gate electrode to expose the upper surface of the dummy gate electrode;

removing the dummy gate electrode to expose a surface of the active region;

forming a gate insulating film on the exposed surface of the active region, the gate insulating film having a thickness not allowing carriers to transmit therethrough by a tunneling phenomenon;

forming a second film on a surface of the first film and on the gate insulating film, the second film being made of conductive material or semiconductor material;

anisotropically etching the second film to leave a side control gate electrode of the second film on a side wall of the first film and to expose a surface of the active region in an area surrounded by the side control gate electrode;

forming a tunneling insulating film on the exposed surface of the active region, the tunneling insulating film having a thinness enough to transmit carriers therethrough by the

tunneling phenomenon, and forming a dielectric film on a side wall of the side control gate electrode, the dielectric film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

forming a third film burying a space surrounded by the side control gate electrode and covering an upper surface of the first film, the third film being made of conductive material or semiconductor material; and

etching back the third film to remove the third film on the first film and to leave a floating gate electrode of the third film in the space surrounded by the side control gate electrode.

Claim 11 (Withdrawn): A method of manufacturing a semiconductor memory, comprising the steps of:

forming an element separation insulating film on a surface of a semiconductor substrate to define an active region surrounded with the element separation insulating film;

forming a tunneling insulating film on the active region of the semiconductor substrate, the tunneling insulating film having a thinness enough to transmit carriers therethrough by a tunneling phenomenon;

forming a first conductive member on the tunneling insulating film, the first conductive film traversing the active region and made of conductive material or semiconductor material;

forming a side wall member on a side wall of the first conductive member;

doping impurities in a surface layer of the active region on both sides of a mesa including the first conductive member and the side wall member;

removing the side wall member;

forming a gate insulating film on upper and side surfaces of the first conductive member and on a partial area of the active region on both sides of the first conductive member, the gate insulating film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

covering a surface of the gate insulating film with a conductive film made of conductive material or semiconductor material; and

anisotropically etching the conductive film to leave a side control gate electrode made of the first conductive film over a side wall of the first conductive member.

Claim 12 (Currently Amended): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness of at most 3nm;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit theretbrough by a direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; ~~and~~

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 13 (Previously Presented): A semiconductor memory according to claim 12, wherein said tunneling insulating film has a thickness of at least 2 mm.

Claim 14 (Currently Amended): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; ~~and~~

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode by a film located above said first and second control gate

electrodes, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein a surface layer of said semiconductor substrate under said first control gate electrode has a conductivity opposite to that of said impurity doped regions, and

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 15 (New): A semiconductor memory according to claim 1, wherein the top surfaces of the impurity doped regions are covered with a metal silicide film, and

the film located above the first and second control gate electrodes is made of the same material as the metal silicide film.

Claim 16 (New): A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said

gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode;

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode;

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode, said second control gate electrode and said floating gate electrode constituting a capacitor,

an element isolation insulating film formed on a partial surface area of the semiconductor substrate and surrounding the pair of impurity doped regions and a channel region between the pair of impurity doped regions; and

a gate bus line over the element isolation insulating film;

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode, and

wherein the first control gate electrode and the second control gate electrode extend on the element isolation insulating film, the gate bus line is in contact with the first control gate electrode and the second control gate electrode over the element isolation insulating film.